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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,944	12/31/2003	Hee Bok Kang	HME-K-0010V	6953

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EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,944	KANG, HEE BOK	
	Examiner	Art Unit	
	David S Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *4-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-9* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the election paper filed 07/07/04.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-3 in the reply filed on 7/7/04 is acknowledged. The traversal is on the ground(s) that the search and examination would not be a serious burden on the examiner. This is not found persuasive because the two species reflect different processing sequence steps and searching for two different methods would cause a serious burden.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 4-9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 07/07/04.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashima (US005903492A) in view of Summerfelt (US005585300A) and Onishi (US005708284A).

Takashima teaches all of the positive steps of claims 1-3 except for forming a ferro-electric film on the sides of the first electrode and a barrier layer metal disposed between the film and wordlines. Takashima teaches a method for forming a NAND type non-volatile ferro-electric memory cell (column 4 line 3) by forming N number of wordlines (WL00-WL13, BS00,1, figure 5A) on a first conduction type semiconductor (column 25 line 55), forming ferro-electric capacitor first electrodes over the wordlines (SNnn (nn odd) and CF 1-3, figure 6A), forming source and drain regions in the substrate on both sides of the ferro-electric capacitor (figure 5A, column 25 lines 57-58), forming ferro-electric second capacitors on the ferro-electric films (SNnn even), forming plugs (PL) for connecting the source and drain regions to the ferro-electric capacitor second electrodes adjacent to the source and drain regions, excluding the first and Nth region of the N numbers of the source and drain (figure 6B) and forming bit lines (BL) on the substrate inclusive of the plugs with an insulating layer (see figure 6B, insulating layer shown, not labeled) disposed in between for electrically connecting the first region and the Nth region (figure 6B).

Takashima does not show the ferro-electric film formed on the sides of the first electrode nor a barrier metal layer disposed between the film and the wordlines.

Summerfelt teaches forming ferro-electric film (38) on the top and sides of a first electrode (36) and to form a barrier film to improve properties of the capacitor (figure 8, Table column 12-15, and column 1 lines 59-61). Onishi teaches to use a metal (8A, figure 1) as a diffusion barrier to provide a highly reliable (improved reliability) memory (column 4 lines 40-44).

Regarding claim 2, Takashima forms a gate insulating film on the first conduction type semiconductor substrate (column 25 line 55, transistor fabrication includes gate insulator between gate and substrate, otherwise the gate is shorted to the substrate), forms wordline material on the gate (WL), in view of Summerfelt and Onishi (as recited above0 forms a barrier metal layer on the wordline material, forms a capacitor electrode material on the barrier metal layer (SN), and selectively removes capacitor material, barrier layer material, wordline material, and gate insulating film to form wordlines insulated from the substrate by the gate insulating fill, (figure 6b shows the result of selectively removing, layers and films have definite side boundaries, the result of deposition and selective removal.) first electrodes (PL) are formed with barrier metal layer between the first electrodes and the wordlines (in view of Summerfelt and Onishi).

Regarding claim 3, a space exists between every adjacent wordline with an insulating material until the sides of the barrier metal layer are exposed (figure 6B shows insulating space between every adjacent wordline. In light of Summerfelt

and Onishi, a barrier metal layer would be on the sides of the first electrodes, thus the barrier metal layer sides are exposed (to at least the insulating material).

It would be obvious to one skilled in the requisite art at the time of the invention would modify Takashima by including a ferro-electric film and a barrier metal layer as taught by Summerfelt to improve properties of the capacitor (figure 8, Table column 12-15, and column 1 lines 59-61) and Onishi to provide a highly reliable (improved reliability) memory (column 4 lines 40-44).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum
July 21, 2004